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EXAMINER	
NGHIEM, MICHAEL P	
ART UNIT	**PAPER NUMBER**
2863	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,473	HOULIHANE, THOMAS SEAN	
	Examiner	Art Unit	
	Michael P. Nghiem	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007 and 14 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14,16-25 and 27-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-14,16,17,19,20,22-25,27-33,35-38,40,41,43,44 and 46* is/are rejected.

7)☒ Claim(s) *10,15,18,21,34,39,42 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Amendment filed on January 22, 2007 has been acknowledged.

Withdrawal of Allowability

The indicated allowability of claims 2 (cancelled, now in claim 1), 3, 4, 23, 26 (cancelled, now in claim 25), 27, 28, and 46 is withdrawn in view of the new ground of rejections.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

"Comprises" (line 6) is an improper legal phraseology.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because lines, numbers, and letters are not uniformly thick and well defined. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-9, 11-14, 16-17, 19-20, 22-25, 27-33, 35-38, 40-41, 43-44, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Nightingale (US 6, 876,941).

Regarding claim 1, Nightingale teaches (a) receiving the configuration data used to configure the representation of the device (column 3, lines 12-15); and (b) generating

the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20 and Ref. 300); (c) generating the representation of the device (column 4, lines 8-10) with reference to the configuration data (column 4, lines 3, 8) and a second set of templates (each configuration file template having entries specific to the device, column 4, lines 6-8, suggests plural sets of templates) defining the representation of the device (column 4, lines 3-10).

Regarding claim 3, Nightingale teaches providing a processing tool having access to the configuration data and the first and second sets of templates, said steps (b) and (c) being performed by the processing tool (column 6, line 49).

Regarding claim 4, Nightingale teaches that the processing tool is operable independent of a language produced by the processing tool from each template (column 6, lines 32-33).

Regarding claim 5, Nightingale teaches that the representation of the device is provided in a first language type and at said step (b) a part of the testbench defined by a number of the templates in the first set is generated in a second language type different to the first language type (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 6, Nightingale teaches that the first language type is a Register Transfer Language (RTL), and the second language type is a High level Verification

Language (HVL) (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 7, Nightingale teaches that the device is a bus interconnect block (see Figure 1).

Regarding claim 8, Nightingale teaches employing a simulation tool to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a master template defining a master engine coupled to a bus and operable during running of the model to generate test stimuli for input via the bus to the representation of the device (column 4, lines 10-12).

Regarding claim 9, Nightingale teaches that the master template includes a master monitor operable during running of the model to monitor signals on the bus to which the master engine is coupled (column 2, lines 16-19 and column 12, lines 6-10).

Regarding claim 11, Nightingale teaches that the master template includes a checker operable during running of the model to check that signals at an interface between the master engine and the bus to which the master engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 12, Nightingale teaches that the master engine is arranged to generate the test stimuli in a random manner (column 20, lines 49-51).

Regarding claim 13, Nightingale teaches employing a simulation tool to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a slave template defining a slave engine coupled to a bus and operable during running of the model to generate response signals in reply to test stimuli received from the representation of the device (column 4, lines 10-12).

Regarding claim 14, Nightingale teaches that the slave template includes a slave monitor operable during running of the model to monitor signals on the bus to which the slave engine is coupled (column 12, lines 6-10).

Regarding claim 16, Nightingale teaches that the slave template includes a checker operable during running of the model to check that signals at an interface between the slave engine and the bus to which the slave engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 17, Nightingale teaches that the slave engine is arranged to generate the response signals in a random manner (column 20, lines 49-51).

Regarding claim 19, Nightingale teaches that there are a number of different component types, and the predetermined attributes specified by the configuration data indicate the component type for each of said one or more components (column 4, lines 3-8).

Regarding claim 20, Nightingale teaches that the device is a bus interconnect block, and wherein one of the component types is a master type, and for each of said one or more components which is a master type, the predetermined attributes identify connections to any slave components within said one or more components that that master type component is connected to (column 3, lines 44-50).

Regarding claim 22, Nightingale teaches a computer program product comprising code portions operable to control a computer to perform a method as claimed in claim 1 (column 9, lines 60-67).

Regarding claim 23, Nightingale teaches (a) receiving a configuration data specifying predetermined attributes of the one or more components (column 3, lines 12-15); (b) employing a processing tool to generate the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20, column 6, line 49); and (c) employing the processing tool to generate the representation of the device (column 4, lines 8-10) with reference to the configuration data (column 4, lines 3, 8) and a second set of templates (each configuration file template having entries specific to the device, column 4, lines 6-8, suggests plural sets

of templates) defining the representation of the device (column 4, lines 3-10).

Regarding claim 24, Nightingale teaches a computer readable medium encoded with computer program product comprising code portions operable to control a computer to perform a method as claimed in claim 23 (column 9, lines 60-67).

Regarding claim 25, Nightingale teaches logic operable to read the configuration data used to configure the representation of the device (column 3, lines 12-15); and generation logic operable to generate the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20 and Ref. 300) and to generate the representation of the device (column 4, lines 8-10) with reference to the configuration data (column 4, lines 3, 8) and a second set of templates (each configuration file template having entries specific to the device, column 4, lines 6-8, suggests plural sets of templates) defining the representation of the device (column 4, lines 3-10).

Regarding claim 27, Nightingale teaches a processing t0ol having access to the configuration data and the first and second sets of templates, the generation logic being provided by the processing tool (column 6, line 49).

Regarding claim 28, Nightingale teaches that the processing tool is operable independent of a language produced by the processing tool from each template (column

6, lines 32-33).

Regarding claim 29, Nightingale teaches that the representation of the device is provided in a first language type, and during generation of the testbench by the generation logic a part of the testbench defined by a number of the templates in the first set is generated in a second language type different to the first language type (column 6, lines 34-36 and column 11, lines 15- 21).

Regarding claim 30, Nightingale teaches that the first language type is a Register Transfer Language (RTL), and the second language type is a High level Verification Language (HVL) (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 31, Nightingale teaches that the device is a bus interconnect block (see Fig. 1).

Regarding claim 32, Nightingale teaches a simulation tool operable to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a master template defining a master engine coupled to a bus and operable during running of the model to generate test stimuli for input via the bus to the representation of the device (column 4, lines 10-12).

Regarding claim 33, Nightingale teaches that the master template includes a master monitor operable during running of the model to monitor signals on the bus to which the master engine is coupled (column 2, lines 16-19 and column 12, lines 6-10).

Regarding claim 35, Nightingale teaches that the master template includes a checker operable during running of the model to check that signals at an interface between the master engine and the bus to which the master engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 36, Nightingale teaches that the master engine is arranged to generate the test stimuli in a random manner (column 20, lines 49-51).

Regarding claim 37, Nightingale teaches a simulation tool operable to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a slave template defining a slave engine coupled to a bus and operable during running of the model to generate response signals in reply to test stimuli received from the representation of the device (column 4, lines 10-12).

Regarding claim 38, Nightingale teaches that the slave template includes a slave monitor operable during running of the model to monitor signals on the bus to which the

slave engine is coupled (column 12, lines 6-10).

Regarding claim 40, Nightingale teaches that the slave template includes a checker operable during running of the model to check that signals at an interface between the slave engine and the bus to which the slave engine is coupled conform to a protocol for that bus.

Regarding claim 41, Nightingale teaches that the slave engine is arranged to generate the response signals in a random manner (column 20, lines 49-51).

Regarding claim 43, Nightingale teaches that there are a number of different component types, and the predetermined attributes specified by the configuration data indicate the component type for each of said one or more components (column 4, lines 3-8).

Regarding claim 44, Nightingale teaches that the device is a bus interconnect block, and wherein one of the component types is a master type, and for each of said one or more components which is a master type, the predetermined attributes identify connections to any slave components within said one or more components that that master type component is connected to (column 3, lines 44-50).

Regarding claim 46, Nightingale teaches logic operable to read a configuration data specifying predetermined attributes of the one or more components (column 3, lines 12-

15); a processing tool operable to generate the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20 and column 6, line 49); and the processing tool further being operable to generate the representation of the device (column 4, lines 8-10) with reference to the configuration data (column 4, lines 3, 8) and a second set of templates (each configuration file template having entries specific to the device, column 4, lines 6-8, suggests plural sets of templates) defining the representation of the device (column 4, lines 3-10).

Allowable Subject Matter

Claims 10, 15, 18, 21, 34, 39, 42, and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of. the base claim and any intervening claims.

The combination as claimed wherein the representation of the device is formed from constituent blocks and the second set of templates defines the representation of the device and its constituent blocks (claims 18, 42) is not disclosed, suggested, or made obvious by the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: Please see previous office action and applicant's remarks for reasons for allowance of claims 10, 15, 21, 34, 39, 42, and 45.

Response to Arguments

Applicant's arguments filed on January 22, 2007 and September 14, 2006 have been fully considered but they are not persuasive.

With respect to claims 1, 23, 25, and 46, Applicant argues that Nightingale does not teach the limitation of generating the representation of the device with reference to the configuration data and a second set of templates defining the representation of the device. Column 3, lines 15-20; column 6, line 49 do not describe a second set of templates nor do they refer to the device to be tested being configurable in any respect.

Examiner's position is that Nightingale discloses generating the representation of the device (column 4, lines 8-10) with reference to the configuration data (column 4, lines 3, 8) and a second set of templates (each configuration file template having entries specific to the device, column 4, lines 6-8, suggests plural sets of templates) defining the representation of the device (column 4, lines 3-10).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael P Nghiem whose telephone number is (571) 272-2277. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL NGHIEM
PRIMARY EXAMINER

Michael Nghiem

September 25, 2007